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| | Filing Date | | 2005-09-23 |
| | First Named Inventor | | Roger D. Chamberlain |
| | Art Unit | | 2439 |
| | Examiner Name | | Tolentino, Roderick |
| | Attorney Docket Number | | 53047-57365 |

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| | 2 | NIEWCZAS ET AL., "A Pattern Matching Algorithm for Verification and Analysis of Very Large IC Layouts", ACM, April 1998, pp. 129-134 | ☐ |
| | 3 | RAMESH ET AL., "Automatic Selection of Tuning Parameters for Feature Extraction Sequences", IEEE, June 21-23, 1994, pp. 672-677 | ☐ |

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